CLAIMS

1. A CMOS inverter comprising:

a heterostructure including a Si substrate, a relaxed $Si_{1-x}Ge_x$ layer on said Si substrate, and a strained surface layer on said relaxed $Si_{1-x}Ge_x$ layer; and

a pMOSFET and an nMOSFET, wherein the channel of said pMOSFET and the channel of said nMOSFET are formed in said strained surface layer.

2. The CMOS inverter of claim 1, wherein the heterostructure further comprises a planarized surface positioned between the strained surface layer and the Si substrate.

3. The CMOS inverter of claim 1, wherein the surface roughness of the strained surface layer is less than 1nm.

4. The CMOS inverter of claim 1, wherein the heterostructure further comprises an oxide layer positioned between the relaxed $Si_{1-x}Ge_x$ layer and the Si substrate.

5. The CMOS inverter of claim 1, wherein the heterostructure further comprises a SiGe graded buffer layer positioned between the relaxed $Si_{1-x}Ge_x$ layer and the Si substrate.

6. The CMOS inverter of claim 1, wherein the strained surface layer comprises Si.

7. The CMOS inverter of claim 1, wherein $0.1 < x < 0.5$.

8. The CMOS inverter of claim 7, wherein the ratio of gate width of the pMOSFET to the gate width of the nMOSFET is approximately equal to the ratio of the electron mobility and the

hole mobility in bulk silicon.

9. The CMOS inverter of claim 7, wherein the ratio of gate width of the pMOSFET to the gate width of the nMOSFET is approximately equal to the ratio of the electron mobility and the hole mobility in the strained surface layer.

10. The CMOS inverter of claim 7, wherein the ratio of gate width of the pMOSFET to the gate width of the nMOSFET is approximately equal to the square root of the ratio of the electron mobility and the hole mobility in bulk silicon.

11. The CMOS inverter of claim 7, wherein the ratio of gate width of the pMOSFET to the gate width of the nMOSFET is approximately equal to the square root of the ratio of the electron mobility and the hole mobility in the strained surface layer.

12. The CMOS inverter of claim 7, wherein the gate drive is reduced to lower power consumption.

13. In a high speed integrated circuit, the CMOS inverter of claim 7.

14. In a low power integrated circuit, the CMOS inverter of claim 7.

15. An integrated circuit comprising:

a heterostructure including a Si substrate, a relaxed $Si_{1-x}Ge_x$ layer on said Si substrate, and a strained layer on said relaxed $Si_{1-x}Ge_x$ layer; and

a p transistor and an n transistor formed in said heterostructure, wherein said strained layer comprises the channel of said n transistor and said p transistor, and said n transistor and

said p transistor are interconnected in a CMOS circuit.

16. The integrated circuit of claim 15, wherein the heterostructure further comprises a planarized surface positioned between the strained layer and the Si substrate.

17. The integrated circuit of claim 15, wherein the surface roughness of the strained layer is less than 1nm.

18. The integrated circuit of claim 15, wherein the heterostructure further comprises an oxide layer positioned between the relaxed $Si_{1-x}Ge_x$ layer and the Si substrate.

19. The integrated circuit of claim 15, wherein the heterostructure further comprises a SiGe graded buffer layer positioned between the relaxed $Si_{1-x}Ge_x$ layer and the Si substrate.

20. The integrated circuit of claim 15, wherein the strained layer comprises Si.

21. The integrated circuit of claim 15, wherein $0.1 < x < 0.5$.

22. The integrated circuit of claim 15, wherein the CMOS circuit comprises a logic gate.

23. The integrated circuit of claim 15, wherein the CMOS circuit comprises a NOR gate.

24. The integrated circuit of claim 15, wherein the CMOS circuit comprises an XOR gate.

25. The integrated circuit of claim 15, wherein the CMOS circuit comprises a NAND gate.

26. The integrated circuit of claim 15, wherein the p-channel transistor serves as a pull-up transistor in said CMOS circuit and the n-channel transistor serves as a pull-down transistor in

said CMOS circuit.

27. The integrated circuit of claim 15, wherein the CMOS circuit comprises an inverter.